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WEST Search History

DATE: Monday, June 28, 2004

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<input type="checkbox"/>	L16	reconfigur\$4 with (data path) with (instruction\$1 or command\$1)	34
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<input type="checkbox"/>	L14	data flow instruction\$1	10
<input type="checkbox"/>	L13	instruction\$1 and L11	6
<input type="checkbox"/>	L12	instruction\$1 with L11	0
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<input type="checkbox"/>	L10	instruction\$1 with L9	50
<input type="checkbox"/>	L9	reconfigur\$4 with (i/o or input/output)	704
<input type="checkbox"/>	L8	programable i/o	5
<input type="checkbox"/>	L7	L6 not l5	6
<input type="checkbox"/>	L6	5970254.uref.	12
<input type="checkbox"/>	L5	6282627.uref.	19
<input type="checkbox"/>	L4	l1 and data path	2
<input type="checkbox"/>	L3	configuration memory and l1	2
<input type="checkbox"/>	L2	(instruction\$1 with data path) and L1	0
<input type="checkbox"/>	L1	wong.in. and (programmable data path).ti.	2

END OF SEARCH HISTORY

WEST Search History

DATE: Monday, June 28, 2004

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END OF SEARCH HISTORY

First Hit Fwd Refs☐

L3: Entry 1 of 2

File: USPT

Aug 28, 2001

US-PAT-NO: 6282627

DOCUMENT-IDENTIFIER: US 6282627 B1

TITLE: Integrated processor and programmable data path chip for reconfigurable computing

DATE-ISSUED: August 28, 2001

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Wong; Dale	San Francisco	CA		
Phillips; Christopher E.	San Jose	CA		
Cooke; Laurence H.	Los Gatos	CA		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Chameleon Systems, Inc.	Sunnyvale	CA			02

APPL-NO: 09/ 446762 [PALM]

DATE FILED: May 25, 2000

PCT-DATA:

APPL-NO	DATE-FILED	PUB-NO	PUB-DATE	371-DATE	102 (E) -DATE
PCT/US98/13565	June 29, 1998	WO99/00739	Jan 7, 1999	May 25, 2000	May 25, 2000

INT-CL: [07] G06 F 13/14

US-CL-ISSUED: 712/15; 712/13

US-CL-CURRENT: 712/15; 712/13

FIELD-OF-SEARCH: 712/37, 712/11, 712/13, 712/15, 712/20

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	<u>5500609</u>	March 1996	Kean	326/41
<input type="checkbox"/>	<u>5535342</u>	July 1996	Taylor	395/307
<input type="checkbox"/>	<u>5535406</u>	July 1996	Kolchinsky	395/800
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<input type="checkbox"/>	<u>5652875</u>	July 1997	Taylor	395/500
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<input type="checkbox"/>	<u>5748979</u>	May 1998	Trimberger	395/800.37
<input type="checkbox"/>	<u>5752006</u>	May 1998	Baxter	395/500
<input type="checkbox"/>	<u>5956518</u>	September 1999	Delton	712/15
<input type="checkbox"/>	<u>5963745</u>	October 1999	Collins	712/13
<input type="checkbox"/>	<u>6023742</u>	February 2000	Ebeling	710/107

ART-UNIT: 273

PRIMARY-EXAMINER: Coleman; Eric

ATTY-AGENT-FIRM: Burns Doane Swecker & Mathis

ABSTRACT:

The present invention, generally speaking, provides a reconfigurable computing solution that offers the flexibility of software development and the performance of dedicated hardware solutions. A reconfigurable processor chip includes a standard processor, blocks of reconfigurable logic (1101, 1103), and interfaces (319a, 319b, 311) between these elements. The chip allows application code to be recompiled into a combination of software and reloadable hardware blocks using corresponding software tools. A mixture of arithmetic cells and logic cells allows for higher effective utilization of silicon than a standard interconnect. More efficient use of configuration stack memory results, since different sections of converted code require different portions of ALU functions and bus interconnect. Many types of interfaces with the embedded processor are provided, allowing for fast interface between standard processor code and configurable "hard-wired" functions.

29 Claims, 30 Drawing figures

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L5: Entry 10 of 19

File: USPT

Nov 11, 2003

US-PAT-NO: 6647511

DOCUMENT-IDENTIFIER: US 6647511 B1

TITLE: Reconfigurable datapath for processor debug functions

DATE-ISSUED: November 11, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Swoboda; Gary L.	Sugarland	TX		
Karthikeyan; Madathil R.	Bangalore			IN
Menon; Amitabh	Bangalore			IN
Matt; David R.	Missouri City	TX		

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
Texas Instruments Incorporated	Dallas	TX			02

APPL-NO: 09/ 379769 [\[PALM\]](#)

DATE FILED: August 24, 1999

PARENT-CASE:

This application claims the benefit of provisional application No. 60/100,712, filed Sep. 17,1998.

INT-CL: [07] [G06 F 11/00](#)US-CL-ISSUED: [714/30](#); [714/733](#), [714/734](#)US-CL-CURRENT: [714/30](#); [714/733](#), [714/734](#)FIELD-OF-SEARCH: [714/723](#), [714/733](#), [714/734](#), [714/30](#), [714/27](#), [714/40](#)

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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	PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
<input type="checkbox"/>	5338984	August 1994	Sutherland	326/41
<input type="checkbox"/>	5974435	October 1999	Abbott	708/523
<input type="checkbox"/>	6058469	May 2000	Baxter	712/43
<input type="checkbox"/>	6282627	August 2001	Wong et al.	712/15
<input type="checkbox"/>	6510530	January 2003	Wu et al.	714/30

ART-UNIT: 2184

PRIMARY-EXAMINER: Beausoliel; Robert

ASSISTANT-EXAMINER: Duncan; Marc

ATTY-AGENT-FIRM: Petersen; Bret J. Brady, III; W. James Telecky, Jr.; Frederick J.

ABSTRACT:

A reconfigurable datapath (13b), which may be alternatively configured for various debug modes. These modes include a breakpoint mode (20), counter mode (30a-30c), DMA mode (40), and PSA mode (50). Each configuration uses one or more of two bitcell units: a register bitcell unit (60) and a comparator bitcell unit (70). The inputs and interconnections of these bitcell units (60, 70) determine the configuration, and hence the mode, for which they are to be used.

32 Claims, 9 Drawing figures

First Hit Fwd Refs



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L5: Entry 10 of 19

File: USPT

Nov 11, 2003

US-PAT-NO: 6647511

DOCUMENT-IDENTIFIER: US 6647511 B1

TITLE: Reconfigurable datapath for processor debug functions

DATE-ISSUED: November 11, 2003

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE
Swoboda; Gary L.	Sugarland	TX	
Karthikeyan; Madathil R.	Bangalore		
Menon; Amitabh	Bangalore		
Matt; David R.	Missouri City	TX	

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Texas Instruments Incorporated	Dallas	TX		

APPL-NO: 09/ 379769 [PALM]

DATE FILED: August 24, 1999

PARENT-CASE:

This application claims the benefit of provisional application No. 60/100,712, filed Sep. 17, 1998.

INT-CL: [07] G06 F 11/00

US-CL-ISSUED: 714/30; 714/733, 714/734

US-CL-CURRENT: 714/30; 714/733, 714/734

FIELD-OF-SEARCH: 714/723, 714/733, 714/734, 714/30, 714/27, 714/40

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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PAT-NO	ISSUE-DATE	PATENTEE-NAME	US-CL
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<input type="checkbox"/> <u>6510530</u>	January 2003	Wu et al.	714/30

Full - [FULL]

Title - [TI]

Citation - [CIT]

Front - [FRO]

Review - [REV]

Classification - [C]

Date - [DATE]

Reference - [REF]

Sequences - [SEQ]

Attachments - [A]

Claims - [CLM]

KWIC - [KWIC]

Drwg Desc - [DRA]

Image - [IMG]

ART-UNIT: 2184

PRIMARY-EXAMINER: Beausoliel; Robert

ASSISTANT-EXAMINER: Duncan; Marc

ATTY-AGENT-FIRM: Petersen; Bret J. Brady, III; W. James Telecky, Jr.; Frederick J.

ABSTRACT:

A reconfigurable datapath (13b), which may be alternatively configured for various debug modes. These modes include a breakpoint mode (20), counter mode (30a-30c), DMA mode (40), and PSA mode (50). Each configuration uses one or more of two bitcell units: a register bitcell unit (60) and a comparator bitcell unit (70). The inputs and interconnections of these bitcell units (60, 70) determine the configuration, and hence the mode, for which they are to be used.

32 Claims, 9 Drawing figures

First Hit Fwd Refs

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L5: Entry 17 of 19

File: USPT

Nov 5, 2002

US-PAT-NO: 6477643

DOCUMENT-IDENTIFIER: US 6477643 B1

**** See image for Certificate of Correction ****

TITLE: Process for automatic dynamic reloading of data flow processors (dfps) and units with two-or-three-dimensional programmable cell architectures (fpgas, dpgas, and the like)

DATE-ISSUED: November 5, 2002

INVENTOR-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY
Vorbach; Martin	Karlsruhe			DE
Munch; Robert	Karlsruhe			DE

ASSIGNEE-INFORMATION:

NAME	CITY	STATE	ZIP CODE	COUNTRY	TYPE CODE
PACT GmbH	Munich			DE	03

APPL-NO: 09/ 613217 [PALM]

DATE FILED: July 10, 2000

PARENT-CASE:

This application is continuation of application Ser. No. 08/947,002 filed Oct. 8, 1997 now U.S. pat. No. 6,088,795.

FOREIGN-APPL-PRIORITY-DATA:

COUNTRY	APPL-NO	APPL-DATE
DE	196 54 846	December 27, 1996

INT-CL: [07] G06 F 9/00

US-CL-ISSUED: 713/100; 710/131, 712/15, 712/223, 713/1

US-CL-CURRENT: 713/100; 710/306, 712/15, 712/223, 713/1

FIELD-OF-SEARCH: 713/100, 713/1, 713/2, 712/220, 712/223, 712/16, 712/10, 712/15, 307/465, 709/221, 709/222, 714/3, 714/7, 395/500, 710/131

PRIOR-ART-DISCLOSED:

U.S. PATENT DOCUMENTS

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<input type="checkbox"/> <u>4739474</u>	April 1988	Holsztynski et al.	

<input type="checkbox"/>	<u>4761755</u>	August 1988	Ardini et al.
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<input type="checkbox"/>	<u>5801715</u>	September 1998	Norman	
<input type="checkbox"/>	<u>5828858</u>	October 1998	Athanas	
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<input type="checkbox"/>	<u>6052773</u>	April 2000	DeHon et al.	
<input type="checkbox"/>	<u>6088795</u>	July 2000	Vorbach et al.	713/100
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<input type="checkbox"/>	<u>6202182</u>	March 2001	Abramovici et al.	
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FOREIGN PATENT DOCUMENTS

FOREIGN-PAT-NO	PUBN-DATE	COUNTRY	US-CL
4416881.0	November 1994	DE	
19654595	July 1998	DE	

19654846	July 1998	DE
19651075	October 1998	DE
0 221 360	May 1987	EP
19704728	May 1987	EP
0428327	May 1991	EP
748 051	December 1991	EP
0539595	May 1993	EP
0 678 985	October 1995	EP
0707269	April 1996	EP
0 726 532	August 1996	EP
735 685	October 1996	EP
0748051	December 1996	EP
0735685	October 1998	EP
A90/04835	May 1990	WO
WO90/11648	October 1990	WO
A 93/11503	June 1993	WO
94/08399	April 1994	WO
95/00161	January 1995	WO
95/26001	September 1995	WO

OTHER PUBLICATIONS

Villasenor, John, et al., "Configurable Computing." Scientific American, vol. 276, No. 6, Jun. 1997, pp. 66-71.

Villasenor, John, et al., "Configurable Computing Solution for Automatic Target Recognition," IEEE, 1996 pp. 70-79.

Athanas, Peter, et al., "IEEE Symposium on FPGAs For Custom Computing Machines," IEEE Computer Society Press, Apr. 19-21, 1995, pp. i-vii, 1-222.

Bittner, Ray, A., Jr., "Wormhole Run-Time Reconfiguration: Conceptualization and VLSI Design of a High Performance Computing system," Dissertation, Jan. 23, 1997, pp. i-xx, 1-415.

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ABSTRACT:

A method for processing data in a configurable unit having a multidimensional cell arrangement a switching table is provided, the switching table including a controller and a configuration memory. Configuration strings are transmitted from the switching table to a configurable element of the unit to establish a valid configuration. A configurable element writes data into the configuration memory.

The controller of the switching table recognizes individual records as commands and may execute the recognized commands. The controller may also recognize and differentiate between events and execute an action in response thereto. In response to an event, the controller may move the position of a pointer, and if it has received configuration data rather than commands for the controller, sends the configuration data to the configurable element defined in the configuration data. The controller may send a feedback message to the configurable element. The configurable element may recognize and analyze the feedback message. An configurable element may transmit data into the configuration memory of the switching table.

11 Claims, 26 Drawing figures